NIRCA MkII for IR Image Sensors

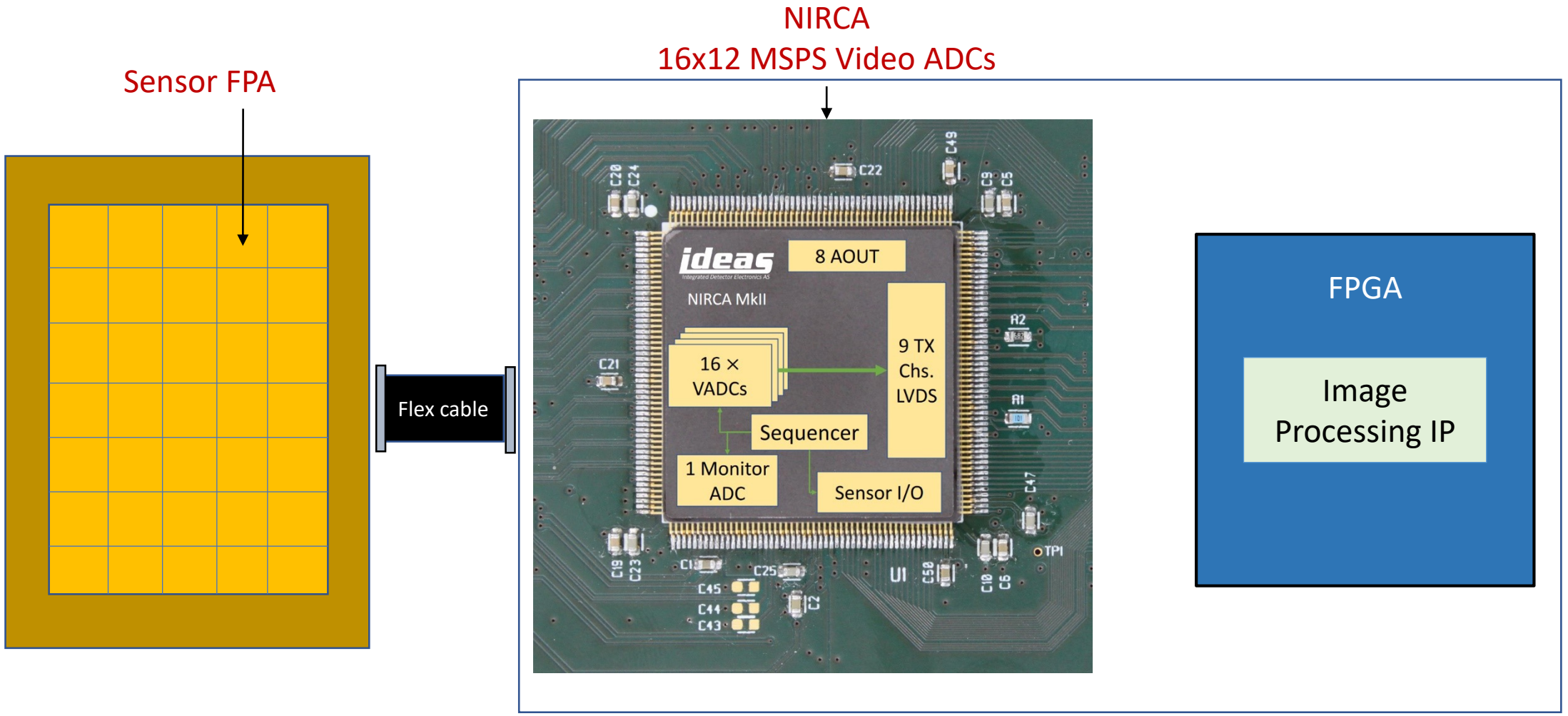
Integrated Detector Electronics (IDEAS)

Workshop: Infrared detection for space applications, Toulouse, 2023

Torbjørn Østmoe

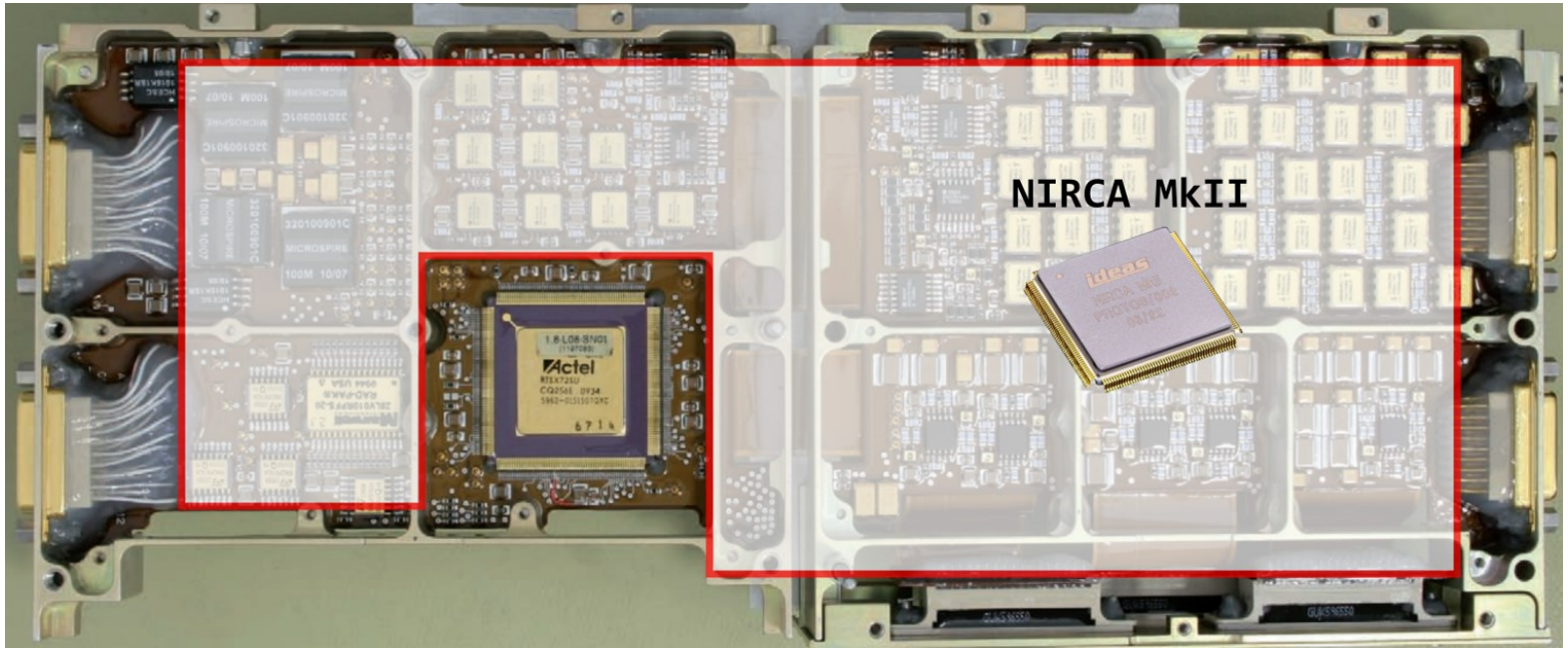
NIRCA – Readout and Controller ASIC for FPA

(Sensor System Block Diagram)



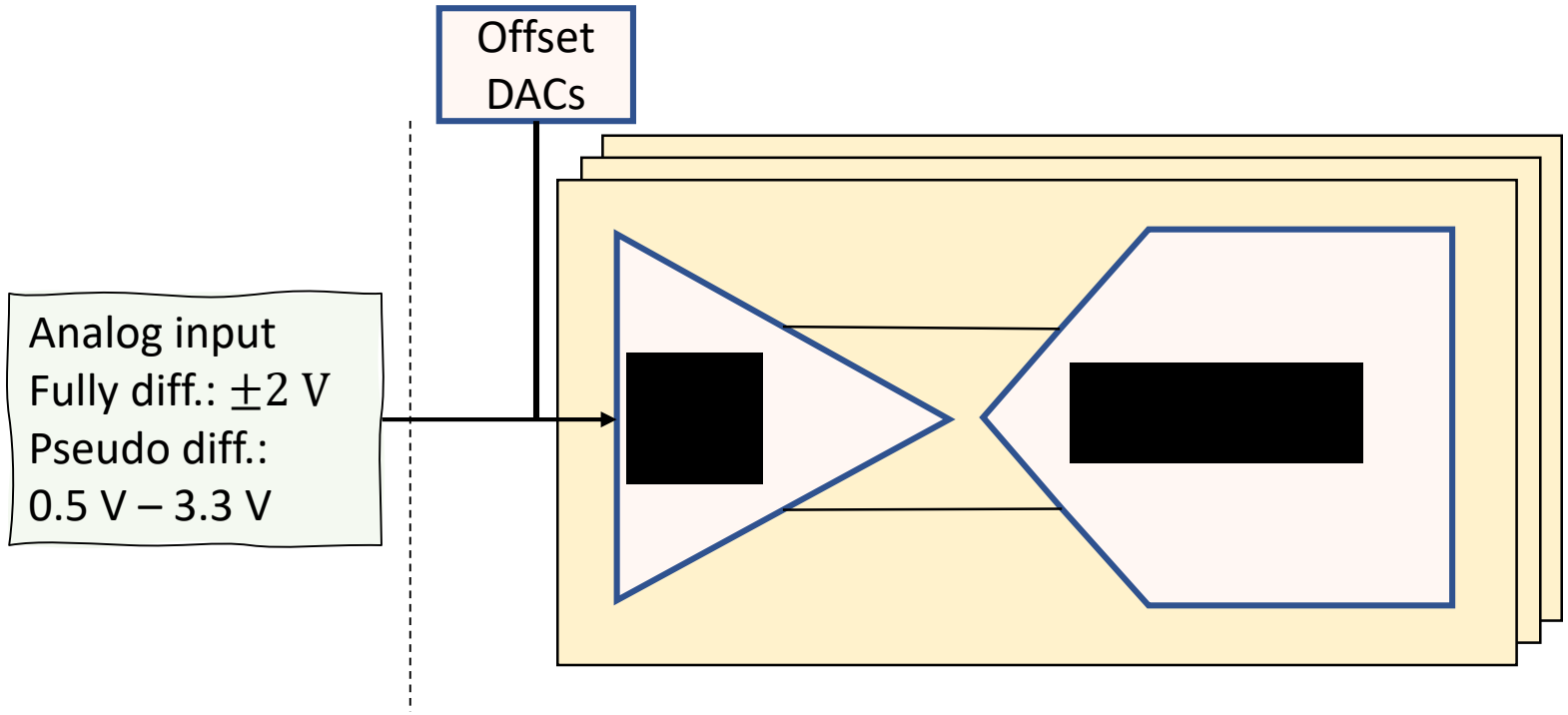
NIRCA Purpose

- **NIRCA** – **N**ear **I**nfrared **R**eadout **C**ontroller **A**SIC – integrates the functions from many discrete components (shaded in figure).
- NIRCA MkII is a single-chip interface between an analog output imaging array and an FPGA
- NIRCA MkII provides:
  - Analog digitization
  - Clock and control
  - Reference, biases and supply
- It reduces design size, weight and power (SWaP), and risk.

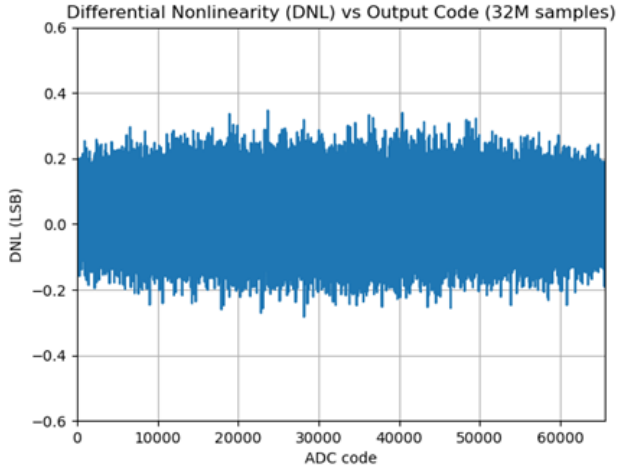


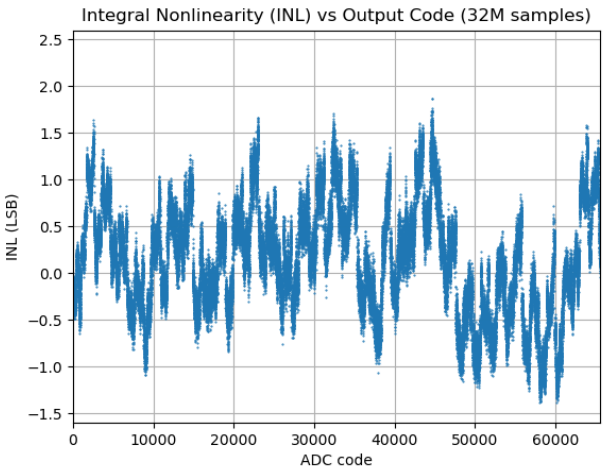
(Sentinel 2-A, MultiSpectral Instrument, front-end electronics)

A/D Converters



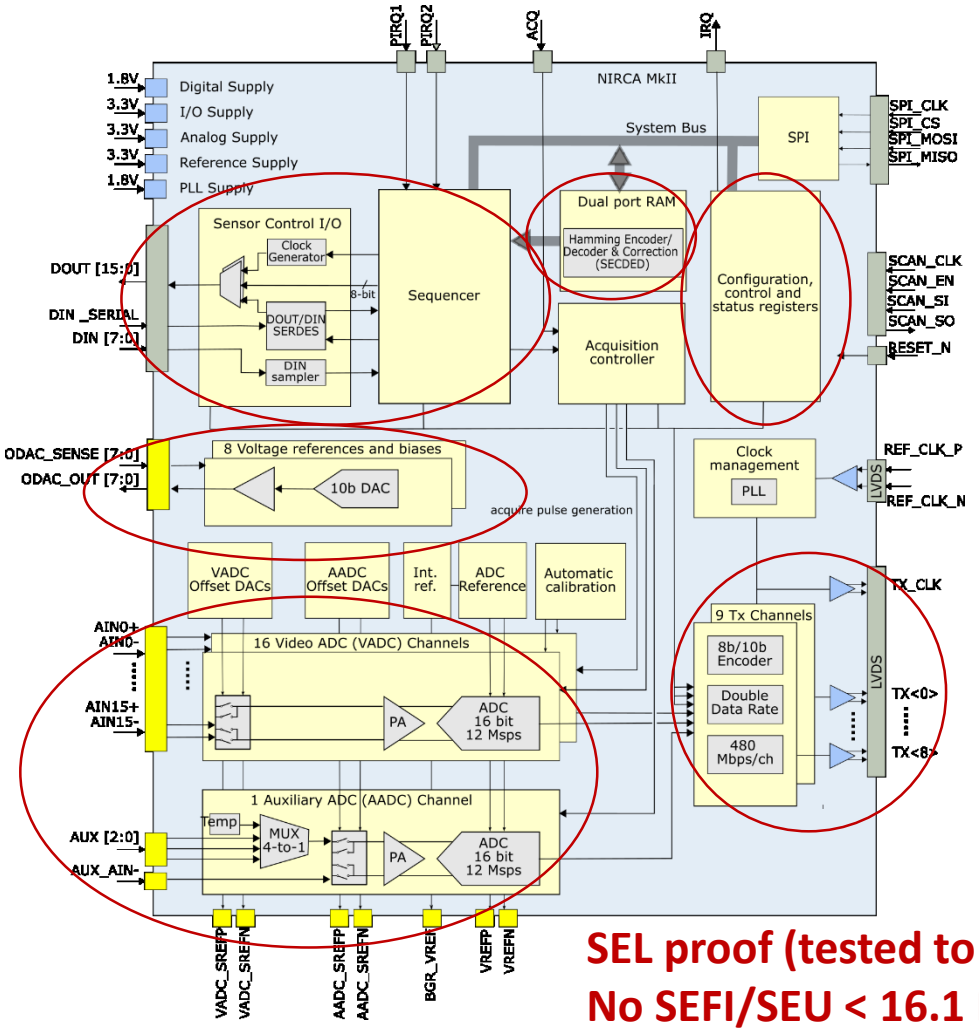
- 16 Video ADCs + 1 monitor ADC
- C_{in} ≈ 10 pF (7 pF sampling capacitor)





Methodology is explained here:
https://www.analog.com/media/en/technical-documentation/tech-articles/histogram-testing-determines-dnl-and-inl-errors.pdf

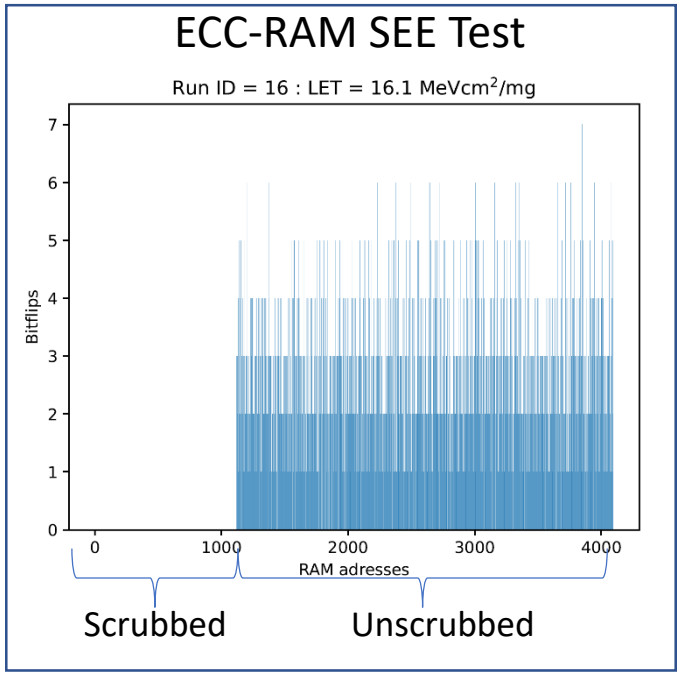
Radiation Hardness

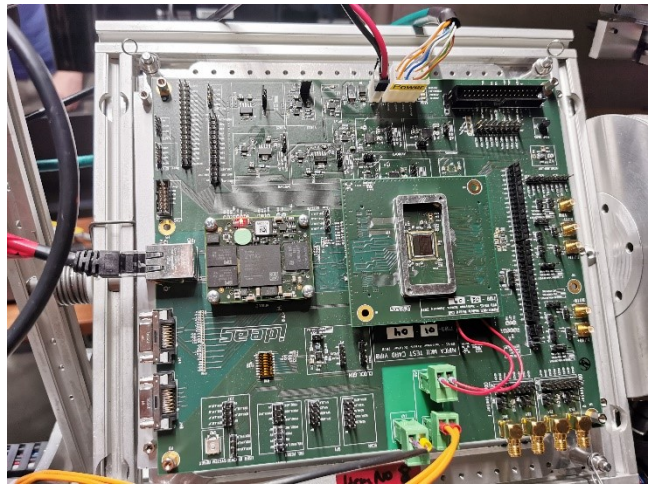


Radiation test highlights

- SEU tolerance of ASIC registers
- Tolerance of TX stream (multiple TX sources)
- SEU tolerance of RAM with and without scrubbing
- Tolerance of digital output waveforms
- Current consumption/SEL test
- ADC performance under TID
- ODAC performance under TID

27 krad low dose rate
+85 krad high dose rate

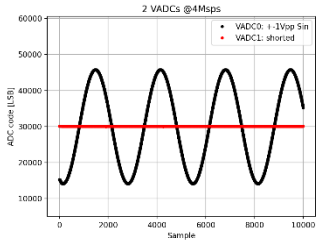




SEL proof (tested to 71.1 MeVcm²/mg)
No SEFI/SEU < 16.1 MeVcm²/mg and few above
No ADC performance drift!

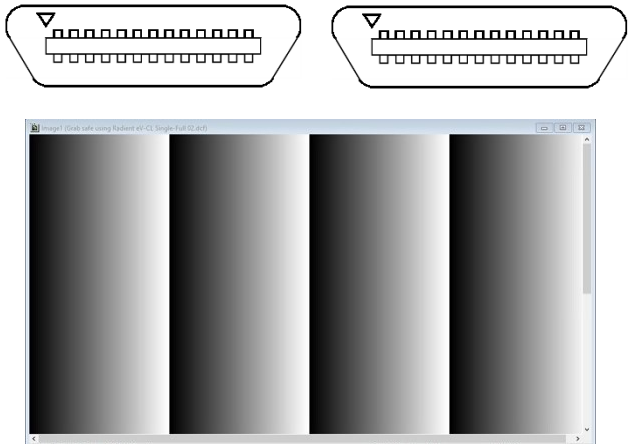
Development Kit

Option 2: Ethernet
1 ADC @12 Msps
2 ADCs @8 Msps
4 ADCs @4 Msps

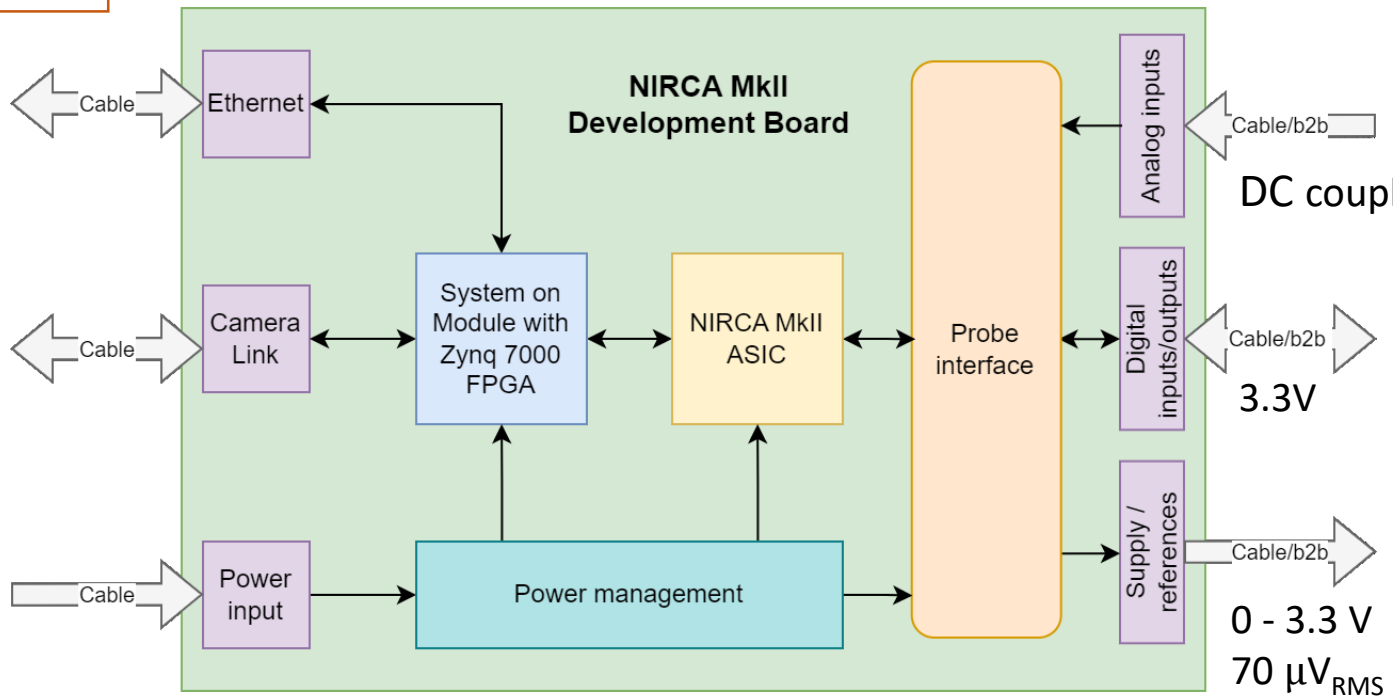


Available in year 2023

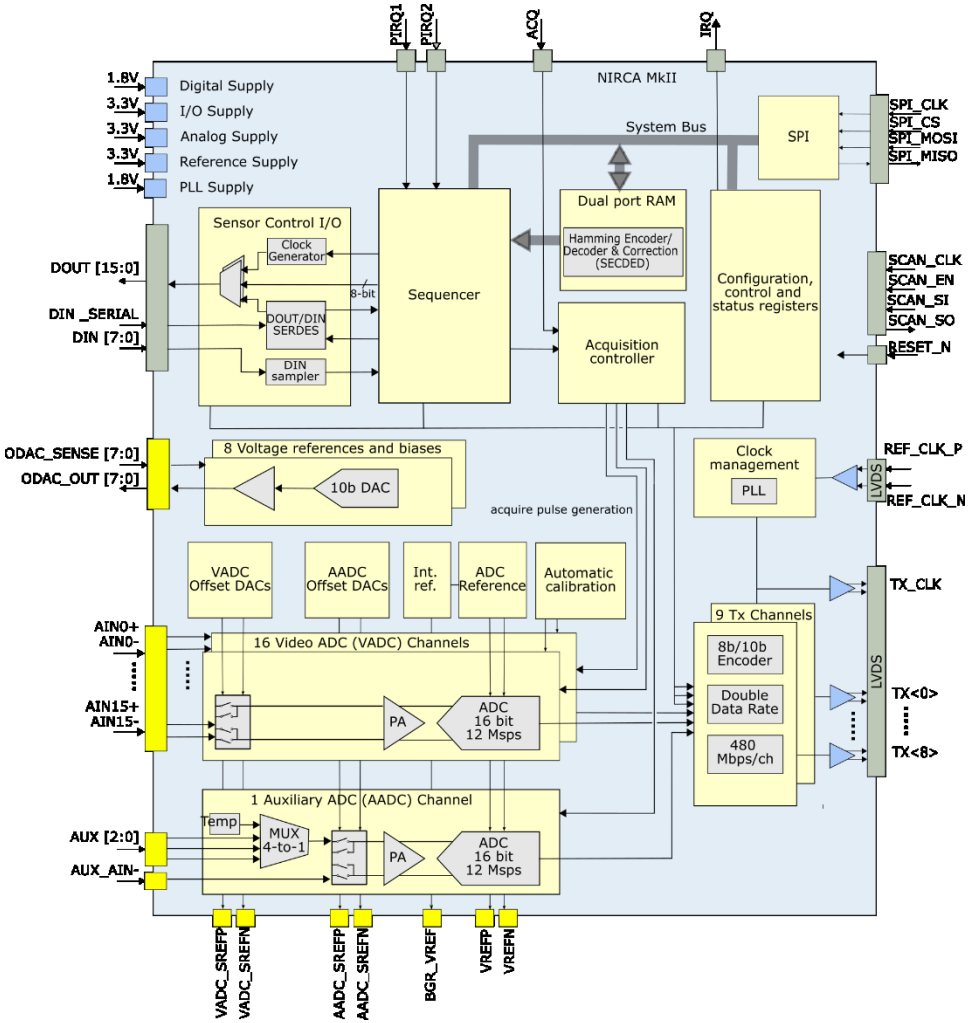
Option 1: CameraLink
All ADCs @12 Msps



Currently integrating the Full CL IP to existing firmware



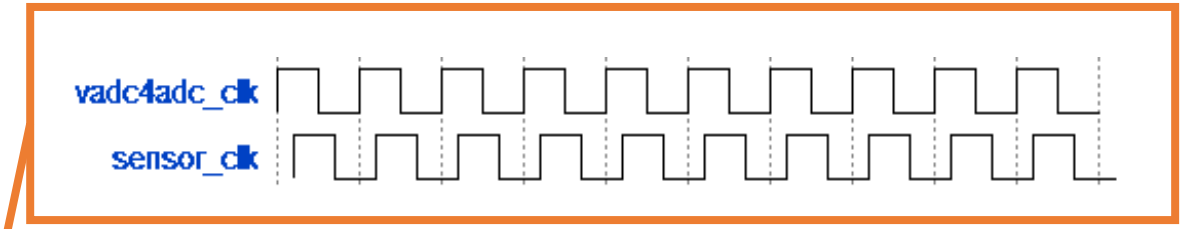
NIRCA Block Diagram

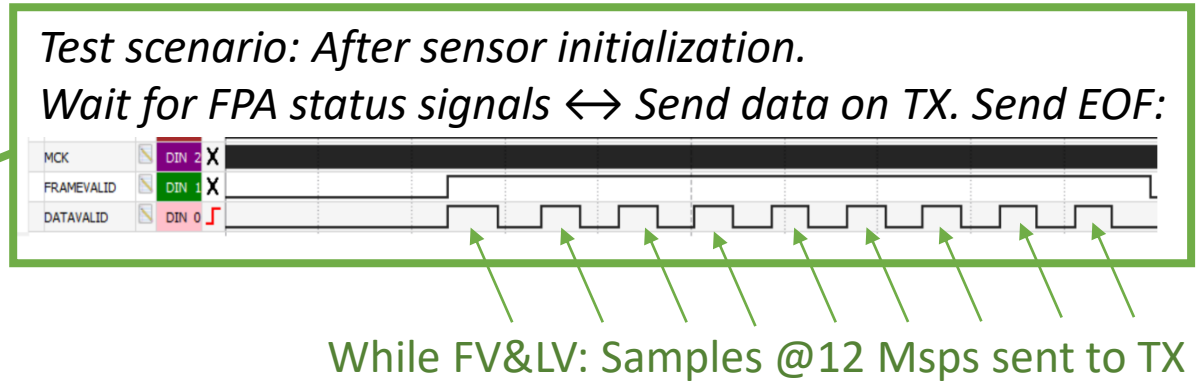


- 16 video channels: preamps + pipeline ADCs max @12 Msps
  - 16-bit mode
  - 14-bit mode + FV/LV
- Monitor ADC, 3 external and 32 internal inputs.
- Programmable sequencer
- SECDED ECC-RAM
- 9 TX channels: LVDS links with 8b/10b encoding. Double data rate @480 Mbps/link. Configurable data source.
- Configuration via SPI interface
- Power consumption 2 W, everything on
- Temperature range: -40 to $+85°C$

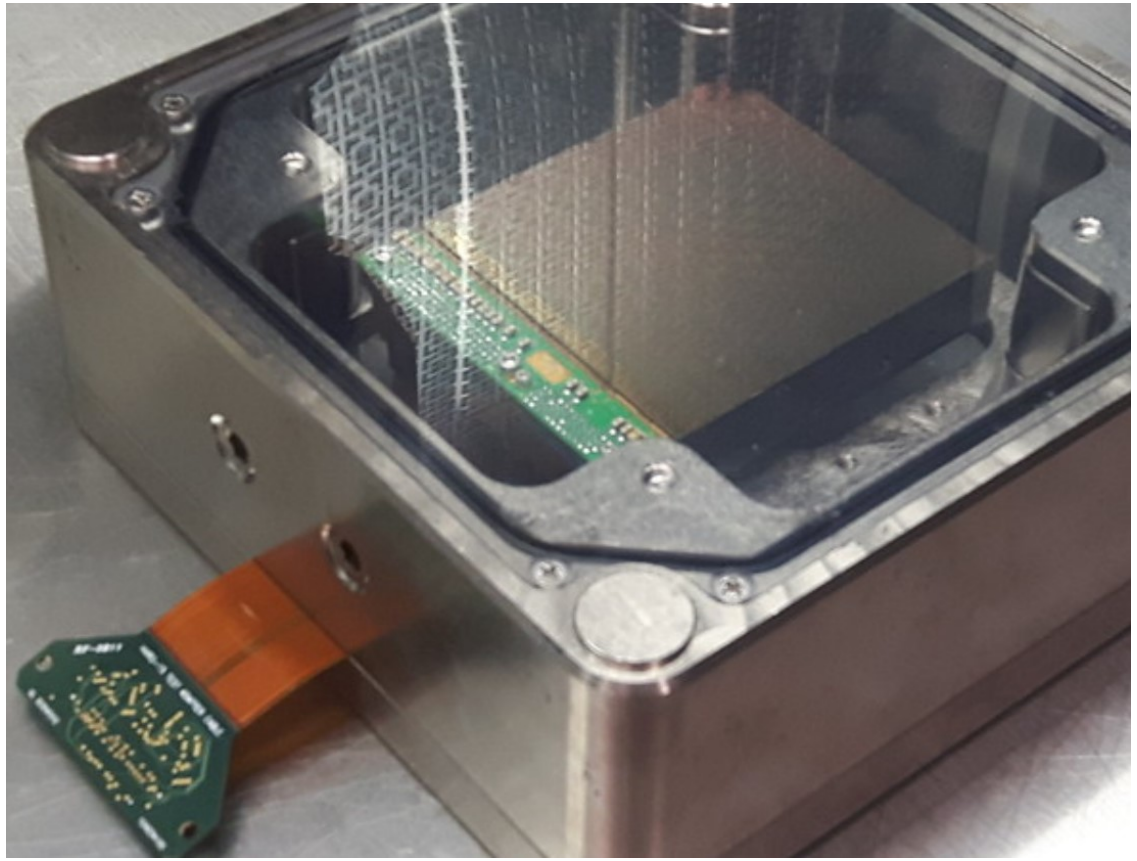
Sequencer Example Operation

1. Reset and program NIRCA MkII using SPI.
2. Establish a link between NIRCA MkII LVDS TX channels and the FPGA RX IP. IDEAS uses a source synchronous receiver IP.
3. Load program into ECC-RAM
4. Generate waveforms at DOUT
   - i.e., waveform to control the image sensor. Output delays is configurable for sampling time control!
5. Start the acquisition
   - Start from the image sensor FV/LV?
   - Run continuously?
   - Based on IRQ?





Use with High-Performance Image Sensors (MCT, InGaAs, InSb)

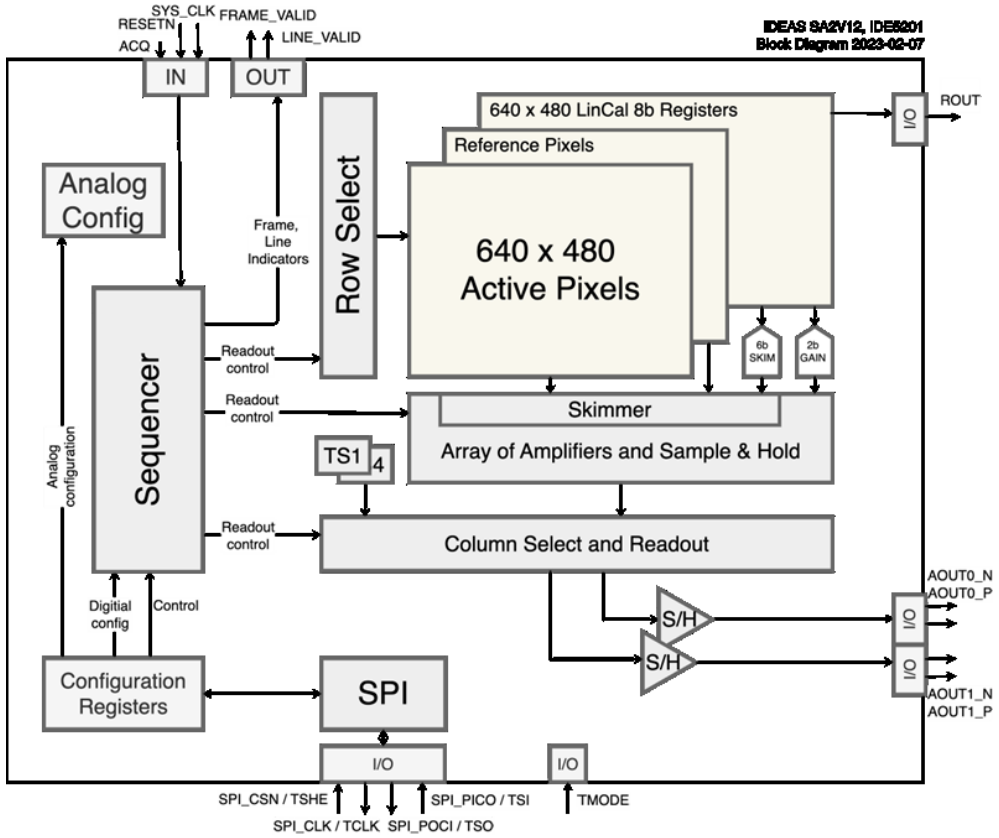


NIRCA is designed to readout high-performance image sensors

Typically, MCT, InGaAs or InSb arrays that needs a cryostat

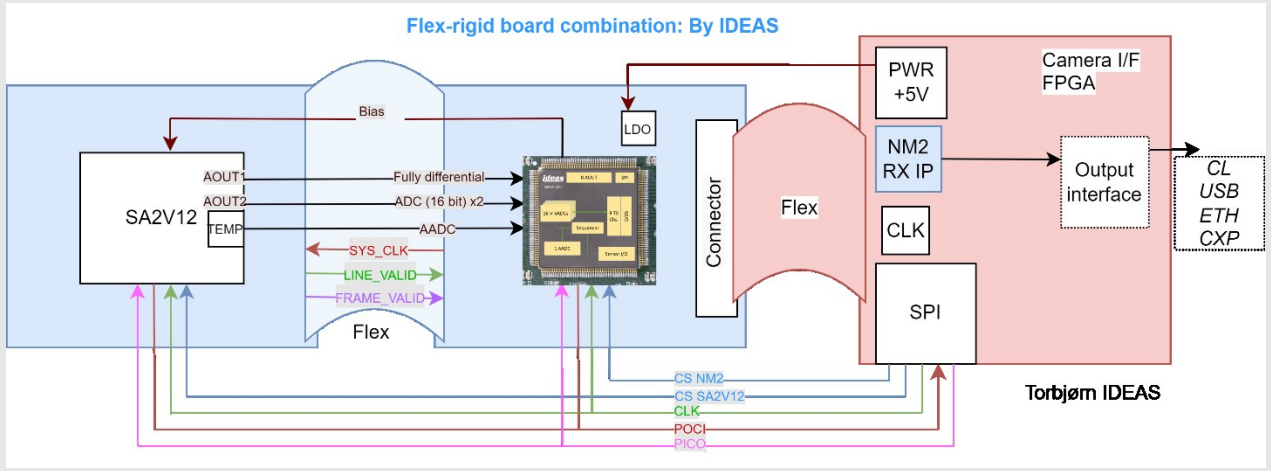
Use with Uncooled Thermal IR Microbolometers

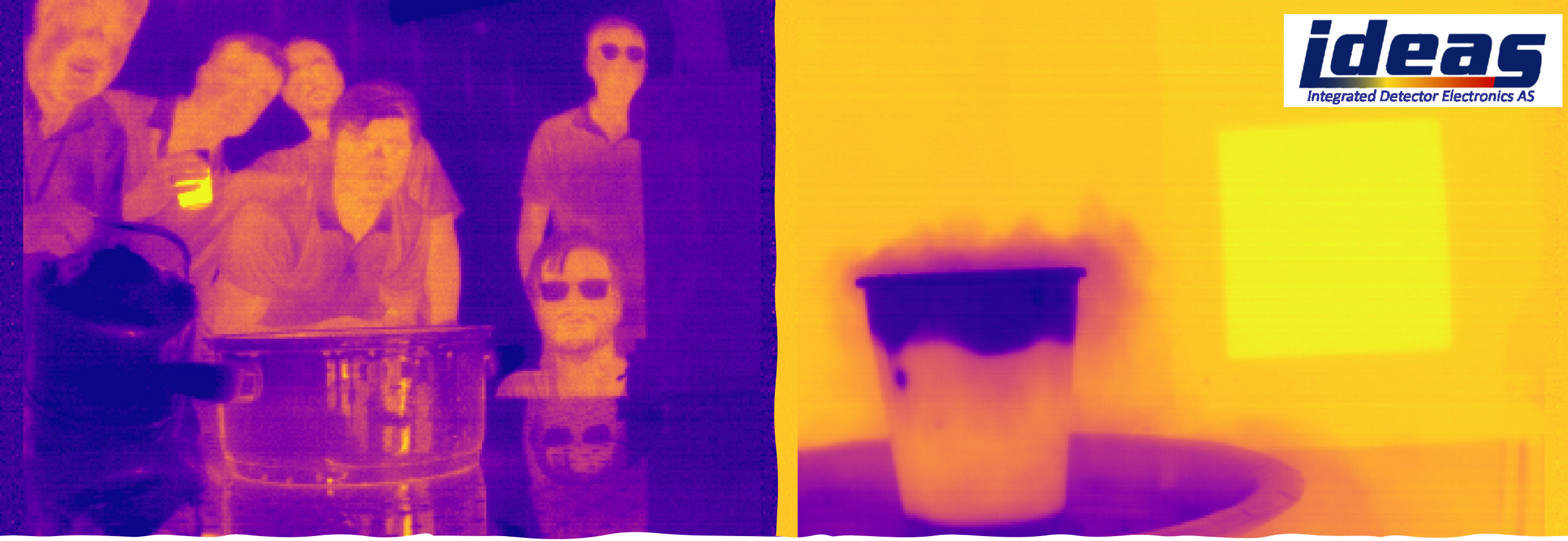
- IDEAS ROIC SA2V12 with Fraunhofer IMS microbolometers, tapeout 2023
- Tailored for use with multispectral pixel sub-arrays
- VGA@60 fps
- On-chip pixel gain calibration (8b/pixel)
- Reference columns for Supply and Temperature drift compensation
- Low power consumption (exp. 60mW)



Thermal IR Camera Demonstrator

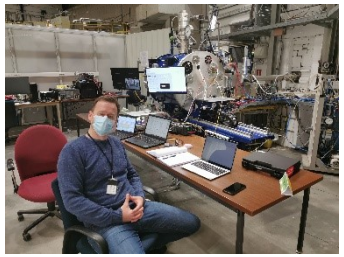
Goal:
Demonstrate NIRCA MkII and SPEKTIR SA2V12 in a compact camera





Thermal IR Demonstrator Test

Contact info



Project manager
amir.hasanbegovic@ideas.no

Presenter
torbjorn.ostmoe@ideas.no

Acknowledgements

esa
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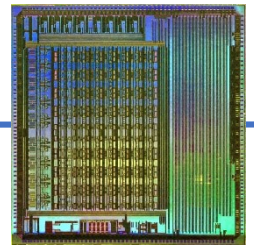
NIRCA MkII status and schedule



Prototype samples available

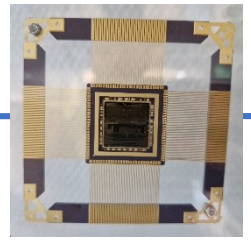
Now

June 23

TBD

ASIC 2nd iteration tapeout

Q4 23



CQFP208 packaging

Q1 24

1. EM samples
2. New radiation tests

2024

3. Qualification (ESCC9000)